

IN THE CLAIMS

Please amend claim 41 as follows below.

Please add new claims 43-58 as follows below.

The following listing of claims replaces all prior versions, and listings, of claims in the application:

1 1-36. (Cancelled)

1 37. (Previously Presented) A pipelined instruction decoder  
2 for a multithread processor, the pipelined instruction decoder  
3 comprising:

4 an instruction decode pipeline to decode instructions  
5 associated with a plurality of instruction threads,  
6 the instruction decode pipeline having a  
7 predetermined number of pipe stages;  
8 a valid bit pipeline in parallel with the instruction  
9 decode pipeline, the valid bit pipeline having the  
10 same predetermined number of pipe stages in parallel  
11 with the predetermined number of pipe stages of the  
12 instruction decode pipeline, the valid bit pipeline  
13 to associate a valid indicator at each pipe stage  
14 with each instruction being decoded in the  
15 instruction decode pipeline; and  
16 a thread identification pipeline in parallel with the  
17 instruction decode pipeline and the valid bit

18 pipeline, the thread identification pipeline having  
19 the same predetermined number of pipe stages in  
20 parallel with the predetermined number of pipe  
21 stages of the instruction decode pipeline and the  
22 valid bit pipeline, the thread identification  
23 pipeline to associate a thread identification at  
24 each pipe stage with each instruction being decoded  
25 in the instruction decode pipeline.

1 38. (Previously Presented) The pipelined instruction  
2 decoder of claim 37 further comprising:  
3 a pipeline controller coupled to the instruction decode  
4 pipeline, the valid bit pipeline, and the thread  
5 identification pipeline, the pipeline controller to  
6 separately control the clocking of each pipe stage  
7 of the instruction decode pipeline, the valid bit  
8 pipeline, and the thread identification pipeline.

1 39. (Previously Presented) The pipelined instruction  
2 decoder of claim 38 wherein  
3 the pipeline controller includes clear logic  
4 for each pipe stage, the clear logic to control the  
5 invalidation of instructions in each pipe stage of  
6 the instruction decode pipeline by setting a valid  
7 bit in a respective pipe stage of the valid bit  
8 pipeline to indicate an invalid instruction.

1 40. (Previously Presented) The pipelined instruction  
2 decoder of claim 38 wherein  
3 the pipeline controller includes  
4 powerdown logic to analyze the valid indicator  
5 of each pipe stage to determine if a next pipe stage  
6 is to be powerdowned and to determine if a pipe  
7 stage is to be stalled; and  
8 clock control logic to determine if respective  
9 clock signals to a pipe stage of the instruction  
10 decode pipeline, the valid bit pipeline, and the  
11 thread identification pipeline are to be stopped to  
12 conserve power or preserve data during a stall.

1 41. (Currently Amended) The pipelined instruction decoder of  
2 claim [[38]] 40 wherein  
3 the powerdown logic of the pipeline controller to analyze  
4 the valid bit of each pipestage to determine if any pipestage  
5 should be stalled,  
6 the powerdown logic including  
7 an exclusive-OR (XOR) gate to exclusively OR a  
8 thread identification of a next to last pipe stage  
9 with a thread identification of a stall to  
10 determined if they match, and  
11 a first AND gate to AND a valid bit of the next  
12 to last pipe stage with an output of the XOR gate,

13                   in order to determine if a pipe stage prior to  
14                   the next to last pipe stage should be stalled.

1    42. (Previously Presented)       The pipelined instruction  
2    decoder of claim 41 wherein  
3       the powerdown logic further including,  
4               a second AND gate to AND the valid indicator of  
5       the pipe stage for which the determination is being  
6       made with the valid indicator of the next pipe  
7       stage, and  
8               a third AND gate to AND an output of the second  
9       AND gate with an output from the first AND gate,  
10       in order to determine if a pipe stage other  
11       than the next to last pipe stage should be stalled.

1    43. (New) The pipelined instruction decoder of claim 38,  
2    wherein  
3       the pipeline controller to squeeze out bubbles of invalid  
4    instructions in the instruction decode pipeline by  
5    continuously clocking a pipestage with an invalid instruction  
6    until a valid instruction is received and overwrites the  
7    invalid instruction.

1    44. (New) The pipelined instruction decoder of claim 38,  
2    wherein

3           the pipeline controller to conserve power by stopping the  
4   clocking of the pipelined instruction decoder if there is no  
5   valid instruction within the pipelined instruction decoder.

1   45. (New) The pipelined instruction decoder of claim 38,  
2   wherein  
3           the pipeline controller to conserve power by stopping the  
4   clocking of circuitry in a pipestage if the thread  
5   indentification associated with the pipestage indicates a  
6   cleared thread of instructions.

1   46. (New) The pipelined instruction decoder of claim 38,  
2   wherein  
3           the pipeline controller includes  
4                   powerdown logic to conserve power.

1   47. (New) The pipelined instruction decoder of claim 38,  
2   wherein  
3                   the pipeline controller to invalidate an entire  
4           thread of instructions in the instruction decode  
5           pipeline associated with a thread identification in  
6           response to a clear signal.

1   48. (New) The pipelined instruction decoder of claim 39,  
2   wherein

3                   the clear logic for each pipe stage of the  
4                   pipeline controller is responsive to a clear signal  
5                   to invalidate an entire thread of instructions in  
6                   the instruction decode pipeline associated with a  
7                   thread identification.

1   49. (New) An apparatus comprising:  
2       an instruction decode pipeline to decode instructions  
3           associated with a plurality of instruction threads,  
4           the instruction decode pipeline having a  
5           predetermined number of pipe stages;  
6       a valid bit pipeline in parallel with the instruction  
7           decode pipeline, the valid bit pipeline having the  
8           same predetermined number of pipe stages in parallel  
9           with the predetermined number of pipe stages of the  
10          instruction decode pipeline, the valid bit pipeline  
11          to associate a valid indicator at each pipe stage  
12          with each instruction being decoded in the  
13          instruction decode pipeline; and  
14       a thread identification pipeline in parallel with the  
15          instruction decode pipeline and the valid bit  
16          pipeline, the thread identification pipeline having  
17          the same predetermined number of pipe stages in  
18          parallel with the predetermined number of pipe  
19          stages of the instruction decode pipeline and the  
20          valid bit pipeline, the thread identification  
21          pipeline to associate a thread identification at

22           each pipe stage with each instruction being decoded  
23           in the instruction decode pipeline; and  
24       a pipeline controller coupled to the instruction decode  
25       pipeline, the valid bit pipeline, and the thread  
26       identification pipeline, the pipeline controller to  
27       squeeze out bubbles of invalid instructions in the  
28       instruction decode pipeline by continuously clocking  
29       a pipestage with an invalid instruction until a  
30       valid instruction is received and overwrites the  
31       invalid instruction.

1   50. (New) The apparatus of claim 49, wherein  
2       the pipeline controller to conserve power by stopping the  
3       clocking of each of the instruction decode pipeline, the valid  
4       bit pipeline, and the thread identification pipeline if there  
5       is no valid instruction within the instruction decode  
6       pipeline.

1   51. (New) The apparatus of claim 49, wherein  
2       the pipeline controller to conserve power by stopping the  
3       clocking of circuitry in a pipestage if the thread  
4       indentification associated with the pipestage indicates a  
5       cleared thread of instructions.

1   52. (New) The apparatus of claim 49, wherein

2       the pipeline controller to invalidate an entire thread of  
3 instructions in the instruction decode pipeline associated  
4 with a thread identification in response to a clear signal.

1   53. (New) A system comprising:

2       a memory; and

3       a microprocessor coupled to the memory, the

4           microprocessor having an instruction decoder, the  
5           instruction decoder including

6                an instruction decode pipeline to decode  
7                instructions associated with a plurality of  
8                instruction threads, the instruction decode  
9                pipeline having a predetermined number of pipe  
10               stages;

11               a valid bit pipeline in parallel with the  
12               instruction decode pipeline, the valid bit  
13               pipeline having the same predetermined number  
14               of pipe stages in parallel with the  
15               predetermined number of pipe stages of the  
16               instruction decode pipeline, the valid bit  
17               pipeline to associate a valid indicator at each  
18               pipe stage with each instruction being decoded  
19               in the instruction decode pipeline; and

20               a thread identification pipeline in  
21               parallel with the instruction decode pipeline  
22               and the valid bit pipeline, the thread  
23               identification pipeline having the same



24                   predetermined number of pipe stages in parallel  
25                   with the predetermined number of pipe stages of  
26                   the instruction decode pipeline and the valid  
27                   bit pipeline, the thread identification  
28                   pipeline to associate a thread identification  
29                   at each pipe stage with each instruction being  
30                   decoded in the instruction decode pipeline.

1   54. (New) The system of claim 53, wherein  
2       the instruction decoder further includes  
3           a pipeline controller coupled to the  
4       instruction decode pipeline, the valid bit pipeline,  
5       and the thread identification pipeline, the pipeline  
6       controller to control the clocking of each pipe  
7       stage of the instruction decode pipeline, the valid  
8       bit pipeline, and the thread identification  
9       pipeline.

1   55. (New) The system of claim 54, wherein  
2       the pipeline controller to squeeze out bubbles  
3       of invalid instructions in the instruction decode  
4       pipeline by continuously clocking a pipestage with  
5       an invalid instruction until a valid instruction is  
6       received and overwrites the invalid instruction.

1 56. (New) The system of claim 54, wherein  
2 the pipeline controller to conserve power by  
3 stopping the clocking to each pipestage of the  
4 instruction decoder if there is no valid instruction  
5 therein.

1 57. (New) The system of claim 54, wherein  
2 the pipeline controller to conserve power by  
3 stopping the clocking of circuitry in a pipestage if  
4 the thread identification associated with the  
5 pipestage indicates a cleared thread of  
6 instructions.

1 58. (New) The system of claim 54, wherein  
2 the pipeline controller to invalidate an entire  
3 thread of instructions in the instruction decode  
4 pipeline associated with a thread identification in  
5 response to a clear signal.